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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,217	02/19/2004	Kevin Nolish	FORE-107	5328

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,217	NOLISH ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on June 18, 2008 for the application of Nolish et al., for a "Method, apparatus and software for preventing switch failures in the presence of faults" filed February 19, 2004.

Claims 1-8, and 10-19 are pending in the application.

Claims 1-8, and 10-19 are rejected under 35 USC § 103.

Claims 6 and 8 have been amended.

Claim Objections

Claim 6 is objected to because of the following informalities:

In claim 6, line 9; "slaver" should be changed to --slave--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (U.S. Patent No. 7,237,146) in view of Azevedo et al. (U.S. Patent No. 6,496,890).

As per claim 1, Suzuki discloses a switch for transferring data (Fig. 1) comprising:

at least one master unit (Fig. 1, element 1, *master device*) a plurality of slave units (Fig. 1, element 2, *slave device*) a bus through which the master unit communicates with the slave units (Fig. 1, element 3)

and a memory (col. 4, lines 15-17) in communication with the master unit having a software program that causes the master unit to automatically recover and restart (col. 4, lines 4-8)

Suzuki fails to explicitly disclose a slave device failure.

Azevedo teaches:

when a slave unit fails which has caused the master unit to fail (col. 7, lines 1-20 and 41-49) and to avoid further accessing the failed slave unit (col. 8, lines 25-31).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of secure data transfer of Suzuki in combination with the bus hang recovery system of Azevedo et al. to effectively detect system failures.

One of ordinary skill in the art at the time of the invention would have been motivated to make the combination because both inventions disclose a method of detecting a failure in a bus system (Suzuki, Fig. 2) and (Azevedo, col. 4, lines 5-10). Both inventions further disclose resetting the system to recover from a failure (Suzuki, col. 4, lines 4-8) and (Azevedo, col. 7, lines 34-40).

As per claim 2, Suzuki discloses persistent storage that survives across abnormal termination of the master unit (col. 4, lines 15-17).

As per claim 3, Suzuki discloses a mechanism for detecting failures of the slave units and thereupon causes the master unit to abnormally terminate (col. 3, lines 30-34) and (col. 4, lines 7-9).

As per claim 4, Suzuki discloses the software program causes the master unit to automatically recover when the detecting mechanism causes the master unit to abnormally terminate (col. 4, lines 7-17).

As per claim 5, Suzuki discloses detecting mechanism includes a hardware watchdog device (col. 4, lines 9-11, expiration of timer).

As per claim 6, Suzuki discloses a method for transferring data comprising the steps of:

attempting to access a failed slave unit (Fig. 2) of a plurality of slave units (Fig. 1, element 2) of a switch by a master unit (Fig. 1, element 1) of the switch with a signal through a bus through which the master unit and the failed slave unit communicate (Fig. 1, element 3)

Suzuki fails to explicitly disclose a slave device failure.

Azevedo teaches:

and automatically recovering and restarting the master unit (col. 7, lines 34-40), which has failed because the failed slave unit failed and caused the master unit to fail (col. 7, lines 1-20 and 41-49) with a software program in the switch that directs the master unit to avoid further accessing the failed slave unit of the plurality of slave units (col. 8, lines 25-31).

As per claim 7, Suzuki discloses the recovering step includes the step of obtaining status information about the slave units from persistent storage (col. 4, lines 15-17).

As per claim 8, Suzuki discloses a software program that is stored on computer readable medium whose contents causes a processor to perform the steps of:

determining a master unit abnormally terminated when the master unit attempted to access a first slave unit which caused the master unit to fail (col. 4, lines 4-8)

Suzuki fails to explicitly disclose a slave device failure.

Azevedo teaches:

restarting the abnormally terminated master unit (col. 7, lines 41-49);

identifying the first slave unit of a plurality of slave units of a switch has failed when the first slave unit is attempted to be accessed by the master unit of the switch (col. 7, lines 1-20); and preventing a master unit from attempting to access the failed first slave unit (col. 8, lines 25-31).

Claims 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (U.S. Patent No. 7,237,146) in view of Azevedo et al. (U.S. Patent No. 6,496,890) and further view of Cepulis et al. (U.S. Patent No. 6,463,550).

As per claim 10, Suzuki in view of Azevedo fails to explicitly disclose changing information in the persistent storage.

Cepulis teaches:

changing information in persistent storage associated with the first slave unit from identified as failed to identified as good if the master unit does not terminate abnormally after the master unit attempts to contact the slave unit (col. 12, lines 62-67 through col. 13, lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of secure data transfer of Suzuki in combination with the fault detection and isolation system of Cepulis et al. to effectively detect system failures.

One of ordinary skill in the art at the time of the invention would have been motivated to make the combination because both inventions disclose a method of

detecting a failure (Suzuki's Fig. 2) and (Cepulis's Fig. 3A) in an I^2C bus system (Suzuki's Fig. 1) and (Cepulis's Fig. 1). Both inventions further disclose persistent memories for data storage (col. 4, lines 15-17 wherein Suzuki discloses "In case the master device 1 is reset, data are read out from memories before conducting a regular processing.") and (col. 4, lines 59-61 wherein Cepulis discloses "If the device fails, the computer system writes an error code or message to the internal memory storage unit.").

As per claim 11, Cepulis discloses the step of setting a variable slot chosen from amongst a plurality of slots of the switch not marked as potentially bad (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 12, Cepulis discloses the step of determining whether the first slave unit is physically present in a first slot of the plurality of slots (col. 8, lines 3-9).

As per claim 13, Cepulis discloses the step of determining the first slot is marked to be skipped (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 14, Cepulis discloses the step of marking the variable slot as potentially bad if it is not marked potentially bad (col. 5, lines 14-20, failed device log)

and (Fig. 5, element 508, tag failed devices).

As per claim 15, Cepulis discloses the step of reporting the variable slot as containing broken hardware (col. 5, lines 14-20, failed device log) and preventing the master unit from attempting to access the variable slot (col. 5, lines 21-34, *prevent access*) if the variable slot is marked to be skipped and (Fig. 5, element 508, tag failed devices).

As per claim 16, Cepulis discloses the step of attempting to access hardware present in the variable slot if the variable slot is marked potentially bad (col. 5, lines 14-20, failed device log) and (Fig. 5, element 508, tag failed devices).

As per claim 17, Cepulis discloses the step of marking the variable slot as good if the switch did not abnormally terminate when the master unit accessed the first slave unit (col. 12, lines 62-67 through col. 13, lines 1-2).

As per claim 18, Cepulis discloses the step of enabling normal operations on hardware present in the variable slot if the variable slot is marked as good (col. 12, lines 62-67 through col. 13, lines 1-2).

As per claim 19, Cepulis discloses the step of setting the variable slot to a next slot of the plurality of slots (Fig. 5, element 516, *check for remaining devices*).

Response to Arguments

Applicant's arguments filed June 18, 2008 with respect to claims 1-8, and 10-19 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Robert W. Beausoliel, Jr./

Supervisory Patent Examiner, Art Unit 2113